74HC237

3-to-8 line decoder, demultiplexer with address latches

Product data sheet

1. General description

The 74HC237 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC237 is specified in compliance with JEDEC standard no. 7A.

The 74HC237 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC237 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 74HC237 acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}1$ and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}1$ is LOW and E2 is HIGH.

The 74HC237 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

2. Features

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V					
	An to Yn			-	16	-	ns
	$\overline{LE}$ to Yn			-	19	-	ns
	$\overline{E}$1 to Yn			-	14	-	ns
	E2 to Yn			-	14	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	60	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC237N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC237D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC237DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16 and SSOP16 packages		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay An to Yn	see Figure 6					
		V_{CC} = 2.0 V		-	52	160	ns
		V_{CC} = 4.5 V		-	19	32	ns
		V_{CC} = 6.0 V		-	15	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	16	-	ns
	propagation delay $\overline{LE}$ to Yn	see Figure 6					
		V_{CC} = 2.0 V		-	61	190	ns
		V_{CC} = 4.5 V		-	22	38	ns
		V_{CC} = 6.0 V		-	18	32	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	19	-	ns
	propagation delay $\overline{E}$1to Yn	see Figure 7					
		V_{CC} = 2.0 V		-	47	145	ns
		V_{CC} = 4.5 V		-	17	29	ns
		V_{CC} = 6.0 V		-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	ns
	propagation delay E2 to Yn	see Figure 6					
		V_{CC} = 2.0 V		-	47	145	ns
		V_{CC} = 4.5 V		-	17	29	ns
		V_{CC} = 6.0 V		-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		V_{CC} = 2.0 V		-	19	75	ns
		V_{CC} = 4.5 V		-	7	15	ns
		V_{CC} = 6.0 V		-	6	13	ns
t_W	$\overline{LE}$ pulse width HIGH	see Figure 8					
		V_{CC} = 2.0 V		50	11	-	ns
		V_{CC} = 4.5 V		10	4	-	ns
		V_{CC} = 6.0 V		9	3	-	ns
t_{su}	set-up time An to $\overline{LE}$	see Figure 8					
		V_{CC} = 2.0 V		50	6	-	ns
		V_{CC} = 4.5 V		10	2	-	ns
		V_{CC} = 6.0 V		9	2	-	ns
t_h	hold time An to $\overline{LE}$	see Figure 8					
		V_{CC} = 2.0 V		30	3	-	ns
		V_{CC} = 4.5 V		6	1	-	ns
		V_{CC} = 6.0 V		5	1	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	60	-	pF

Table 8: Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay An to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	200	ns
		V_{CC} = 4.5 V	-	-	40	ns
		V_{CC} = 6.0 V	-	-	34	ns
	propagation delay $\overline{LE}$ to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	240	ns
		V_{CC} = 4.5 V	-	-	48	ns
		V_{CC} = 6.0 V	-	-	41	ns
	propagation delay $\overline{E}$1 to Yn	see Figure 7				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
	propagation delay E2 to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	$\overline{LE}$ pulse width HIGH	see Figure 8				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_{su}	set-up time An to $\overline{LE}$	see Figure 8				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_h	hold time An to $\overline{LE}$	see Figure 8				
		V_{CC} = 2.0 V	40	-	-	ns
		V_{CC} = 4.5 V	8	-	-	ns
		V_{CC} = 6.0 V	7	-	-	ns

Table 8: Dynamic characteristics *...continued*

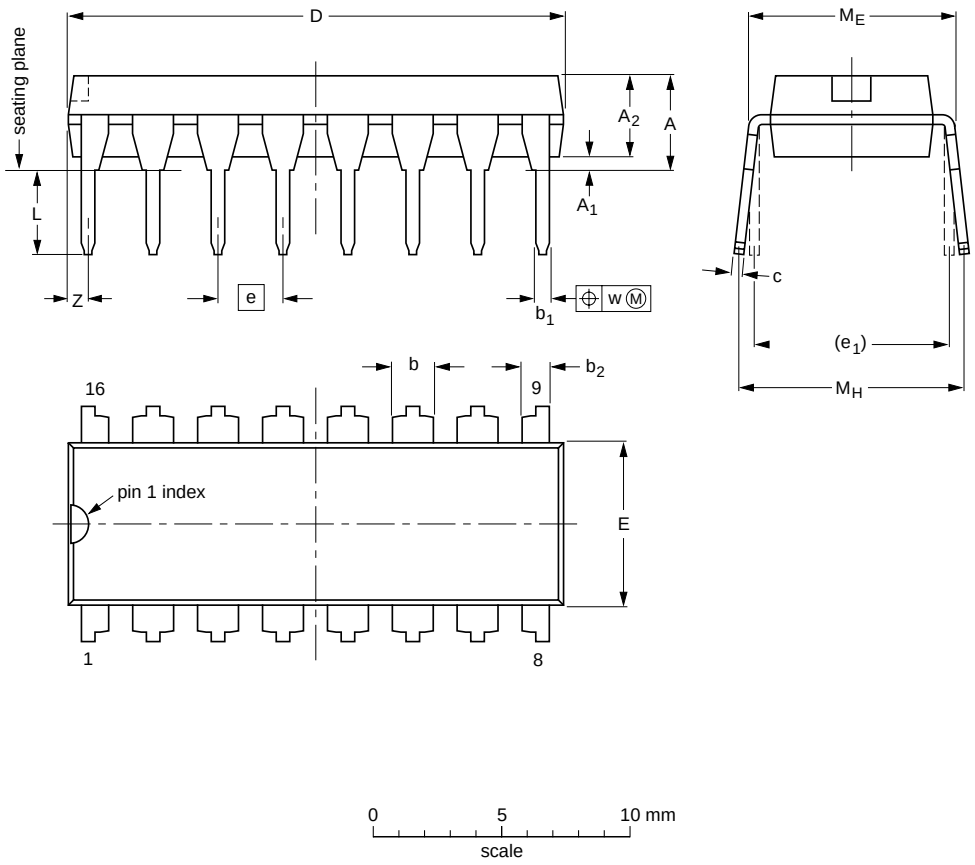
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay An to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	240	ns
		V_{CC} = 4.5 V	-	-	48	ns
		V_{CC} = 6.0 V	-	-	41	ns
	propagation delay $\overline{LE}$ to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	285	ns
		V_{CC} = 4.5 V	-	-	57	ns
		V_{CC} = 6.0 V	-	-	48	ns
	propagation delay $\overline{E}$1 to Yn	see Figure 7				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
	propagation delay E2 to Yn	see Figure 6				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
t_{THL}, t_{TLH}	output transition time	see Figure 7				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	$\overline{LE}$ pulse width HIGH	see Figure 8				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_{su}	set-up time An to $\overline{LE}$	see Figure 8				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_h	hold time An to $\overline{LE}$	see Figure 8				
		V_{CC} = 2.0 V	45	-	-	ns
		V_{CC} = 4.5 V	9	-	-	ns
		V_{CC} = 6.0 V	8	-	-	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-4						

Fig 11. Package outline SOT38-4 (DIP16)